DATA SHEET

SAA4977H
Besic

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Philips
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- Synchronous No parity Eight bit Reception and Transmission (SNERT) interface.

2 GENERAL DESCRIPTION

The SAA4977H is a video processing IC providing analog YUV interfacing, video enhancing features, memory controlling and an embedded 80C51 microprocessor core. It is applicable especially for field rate up-conversion (50 to 100 Hz or 60 to 120 Hz) in cooperation with a 2.9 Mbit field memory. It is designed for applications together with:

SAA4955/56TJ, TMS4C2972/73 (serial field memories)

SAA4990H (PROZONIC)

SAA4991WP (MELZONIC).

3 QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
$V_{DDA(1,2,3)}$	analog supply voltage front-end	4.75	5.0	5.25	V
$V_{DDD(1,2,3)}$	digital supply voltage front-end	4.75	5.0	5.25	V
$V_{DDA(4,5)}$	analog supply voltage back-end	3.15	3.3	3.45	V
$V_{DDD(4,5,6)}$	digital supply voltage back-end	3.15	3.3	3.45	V
V_{DDIO}	I/O supply voltage back-end	3.15	5.0	5.25	V
$I_{DDA(1,2,3)}$	analog supply current front-end	–	85	100	mA
$I_{DDD(1,2,3)}$	digital supply current front-end	–	65	80	mA
$I_{DDA(4,5)}$	analog supply current back-end	–	25	35	mA
$I_{DDD(4,5,6)}$	digital supply current back-end	–	40	55	mA
I_{DDIO}	I/O supply current back-end	–	1	10	mA
P_{tot}	total power dissipation	–	–	1.3	W
T_{amb}	operating ambient temperature	–20	–	+60	°C

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA4977H	QFP80	plastic quad flat package; 80 leads (lead length 1.95 mm); body 14 × 20 × 2.8 mm	SOT318-2

5 BLOCK DIAGRAM

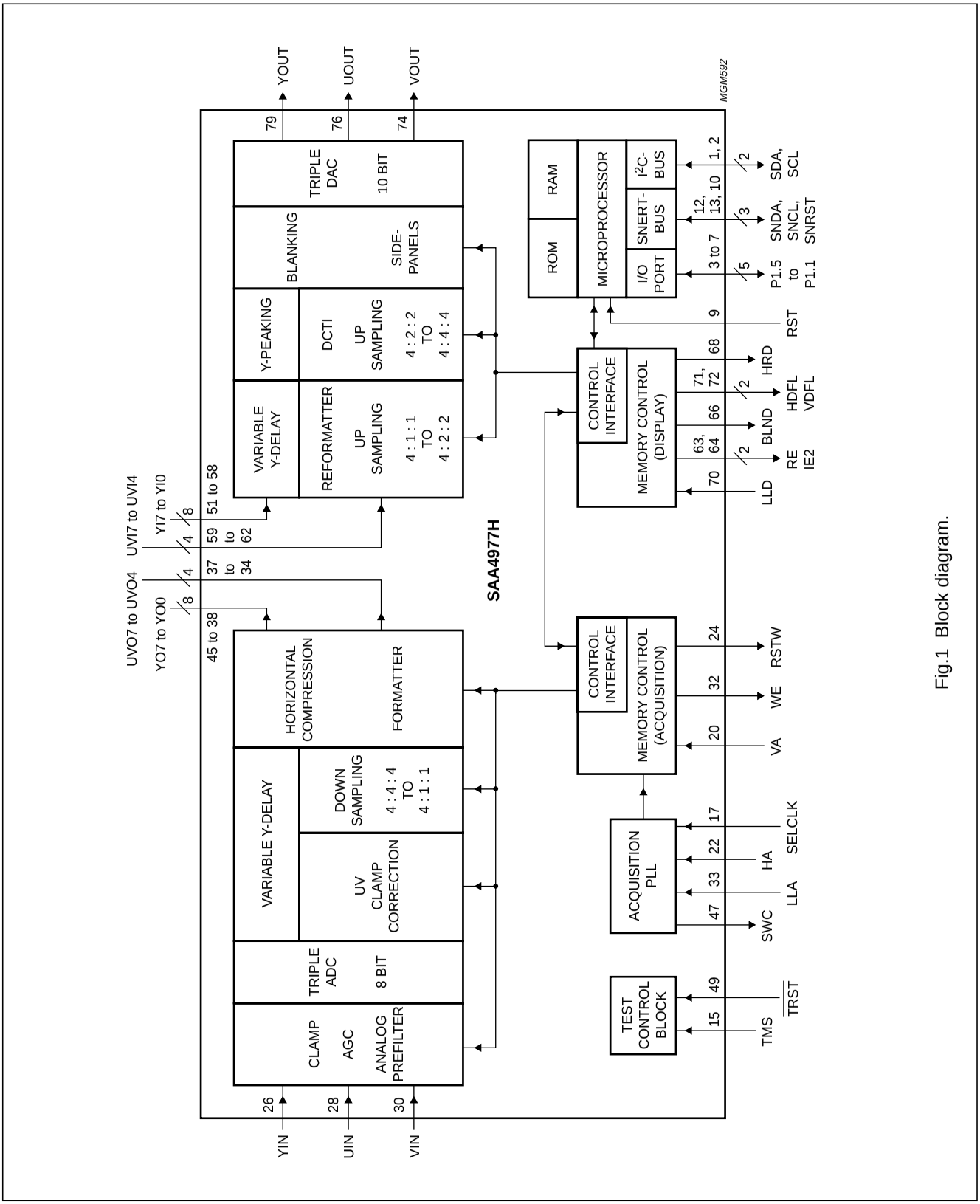


Fig.1 Block diagram.

6 PINNING INFORMATION

6.1 Pinning

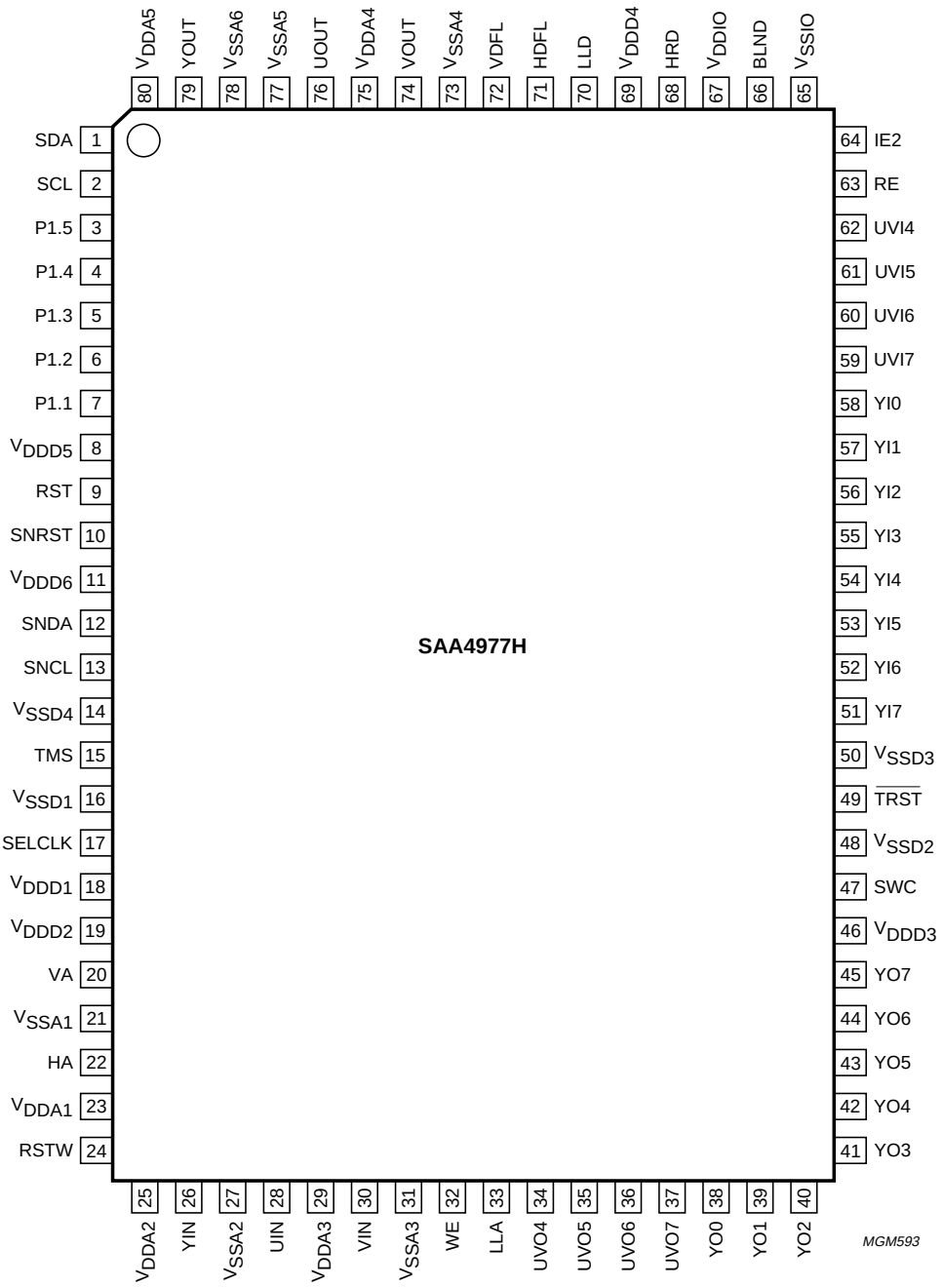


Fig.2 Pin configuration.

6.2 Pin description

Table 1 QFP80 package

SYMBOL	PIN	DESCRIPTION
SDA	1	I^2C-bus serial data (P1.7)
SCL	2	I^2C-bus serial clock (P1.6)
P1.5	3	Port 1 data input/output signal 5
P1.4	4	Port 1 data input/output signal 4
P1.3	5	Port 1 data input/output signal 3
P1.2	6	Port 1 data input/output signal 2
P1.1	7	Port 1 data input/output signal 1
V_{DDD5}	8	digital supply voltage 5 (3.3 V)
RST	9	microprocessor reset input
SNRST	10	SNERT restart (port 1.0)
V_{DDD6}	11	digital supply voltage 6 (3.3 V)
SNDA	12	SNERT data
SNCL	13	SNERT clock
V_{SSD4}	14	digital ground 4
TMS	15	test mode select
V_{SSD1}	16	digital ground 1
SELCLK	17	select acquisition clock input; internal PLL if HIGH, external clock if LOW
V_{DDD1}	18	digital supply voltage 1 (5 V)
V_{DDD2}	19	digital supply voltage 2 (5 V)
VA	20	vertical synchronization input, acquisition part
V_{SSA1}	21	analog ground 1
HA	22	analog/digital horizontal reference input
V_{DDA1}	23	analog supply voltage 1 (5 V)
RSTW	24	reset write signal output, memory 1
V_{DDA2}	25	analog supply voltage 2 (5 V)
YIN	26	Y analog input
V_{SSA2}	27	analog ground 2
UIN	28	U analog input
V_{DDA3}	29	analog supply voltage 3 (5 V)
VIN	30	V analog input
V_{SSA3}	31	analog ground 3
WE	32	write enable signal output, memory 1
LLA	33	acquisition clock input
UVO4	34	V digital output bit 0
UVO5	35	V digital output bit 1
UVO6	36	U digital output bit 0
UVO7	37	U digital output bit 1
YO0	38	Y digital output bit 0

SYMBOL	PIN	DESCRIPTION
YO1	39	Y digital output bit 1
YO2	40	Y digital output bit 2
YO3	41	Y digital output bit 3
YO4	42	Y digital output bit 4
YO5	43	Y digital output bit 5
YO6	44	Y digital output bit 6
YO7	45	Y digital output bit 7 (MSB)
V_{DDD3}	46	digital supply voltage 3 (5 V)
SWC	47	serial write clock output
V_{SSD2}	48	digital ground 2
$\overline{TRST}$	49	test reset, active LOW
V_{SSD3}	50	digital ground 3
YI7	51	Y digital input bit 7 (MSB)
YI6	52	Y digital input bit 6
YI5	53	Y digital input bit 5
YI4	54	Y digital input bit 4
YI3	55	Y digital input bit 3
YI2	56	Y digital input bit 2
YI1	57	Y digital input bit 1
YI0	58	Y digital input bit 0
UVI7	59	U digital input bit 1
UVI6	60	U digital input bit 0
UVI5	61	V digital input bit 1
UVI4	62	V digital input bit 0
RE	63	read enable signal output, memory 1
IE2	64	input enable signal output, memory 2
V_{SSIO}	65	I/O ground
BLND	66	horizontal blanking signal output, display part
V_{DDIO}	67	I/O supply voltage (5 V)
HRD	68	horizontal reference signal output, deflection part
V_{DDD4}	69	digital supply voltage 4 (3.3 V)
LLD	70	display clock input
HDFL	71	horizontal synchronization signal output, deflection part
VDFL	72	vertical synchronization signal output, deflection part
V_{SSA4}	73	analog ground 4
VOUT	74	V analog output
V_{DDA4}	75	analog supply voltage 4 (3.3 V)
UOUT	76	U analog output
V_{SSA5}	77	analog ground 5

SYMBOL	PIN	DESCRIPTION
V_{SSA6}	78	analog ground 6
YOUT	79	Y analog output
V_{DDA5}	80	analog supply voltage 5 (3.3 V)

7 FUNCTIONAL DESCRIPTION

7.1 Analog-to-digital conversion

7.1.1 Clamp circuit, clamping Y to digital level 16 and UV to 0 (2's complement)

A clamp circuit is applied for each input channel, to map the colourless black level in each video line (on the sync back porch) to level 16 for Y and to the centre level of the converters for U and V. During the clamp period, an internally generated clamp pulse is used to switch on the clamp action. An operational transconductance amplifier like construction, which references to voltage reference points in the ladders of the ADCs, will provide a current on the input of the YUV signals, in order to bring the signals to the correct DC value. This current is proportional to the DC error, but is limited to ±100 μA. When the clamping action is off, the residual clamp current should be very low in order not to drift away within a video line.

7.1.2 Gain elements for automatic gain control

A variable amplifier is used to map the possible YUV input range to the ADC range. A rise of 6 dB up to a drop fall of 6 dB w.r.t. the nominal values can be achieved. The gain setting within this range is done digitally via control registers. For this purpose a gain setting DAC is incorporated. The smallest step in the gain setting should be hardly visible on the picture, which can be met with smallest steps of 0.4%/step.

Luminance and chrominance gain settings can be separately controlled. The reason for this split is that U and V may be gain adjusted already, whereas luminance is to be adjusted by the SAA4977H AGC. On the other hand, for RGB originated sources, Y, U and V should be adjusted with the same AGC gain.

7.1.3 Analog anti-aliasing prefiltering

A third order linear phase filter is applied on each of the Y, U and V channels. It provides a notch on f_{CLK} (16 MHz) to strongly prevent aliasing to low frequencies, which would be the most disturbing. The bandwidth of the filters is designed for −3 dB at 5.6 MHz. The filters can be bypassed if external filtering with other characteristics is desired.

7.1.4 Triple 8-bit analog-to-digital conversion

Three identical ADCs are used to convert Y, U and V with 16 MHz data rate. A multi-step type ADC is applied here.

7.2 Digital processing at $1f_H$ level

7.2.1 Overload detection

The overload detection provides information to make efficient use of the AGC. The number of overflows per video field in the luminance channel is accumulated by a 14-bit counter. The 8 MSBs of this counter can be read out by the microprocessor respectively via the I^2C-bus. Overflow levels can be programmed as 216, 224, 232 and 240.

7.2.2 Digital clamp correction for UV

During 32 samples within the clamp position the clamp error is measured and accumulated to make a low-pass filtered value of the clamp error. Then a vertical recursive filter is used to further low-pass this error value. This value can be read by the microprocessor or directly be used to correct the clamp error. It is also possible to give a fixed correction value by the microprocessor.

7.2.3 4 : 4 : 4 to 4 : 1 : 1 down-sampling and UV coring

The U and V samples from the ADC are low-pass filtered, before being subsampled with a factor of 2. Coring is applied to the subsampled signal to obtain no gain for low amplitudes which is considered to be noise. Coring levels can be programmed as 0 (off), ±½, ±1 and ±2 LSB.

The U and V samples from the 4 : 2 : 2 data are low-pass filtered again, before being subsampled a second time with a factor of 2 and formatted to 4 : 1 : 1 format.

7.2.4 Y-delay

The Y samples can be shifted onto 8 positions w.r.t. the UV samples. This shift is meant to account for a possible difference in delay previous to the SAA4977H. The zero delay setting is suitable for the nominal case of aligned input data according to the interface format standard. The other settings provide four samples less delay to three sample more delay in Y.

7.2.5 HORIZONTAL COMPRESSION

For displaying 4 : 3 sources on 16 : 9 screens a horizontal signal compression can be done by data interpolation. Therefore two horizontal compression factors of either $^4/_3$ or $^7/_6$ are possible. Via the I^{2}C-bus the compression can be switched on or off and the compression mode 16 : 9 or 14 : 9 can be selected. When the compression mode is active, a reduced number of the interpolated data is stored in the field memory. To achieve sufficiently high accuracy in interpolation Variable Phase Delay filters are used (VPD10 for luminance, a multiplexed VPD06 for UV).

7.3 Digital processing at $2f_H$ level

7.3.1 4 : 1 : 1 TO 4 : 2 : 2 UP-CONVERSION

An up-converter to 4 : 2 : 2 is applied with a linear interpolation filter for creation of the extra samples. These are combined with the original samples from the 4 : 1 : 1 stream.

7.3.2 DCTI

The Digital Colour Transient Improvement (DCTI) is intended for U and V signals originating from a 4 : 1 : 1 source. Horizontal transients are detected and enhanced without overshoots by differentiating, make absolute and again differentiating the U and V signals separately.

This results in a 4 : 4 : 4 U and V bandwidth. To prevent third harmonic distortion, typical for this processing, a so called over the hill protection prevents peak signals becoming distorted. Via the I^{2}C-bus it is possible to control: gain width (see Fig.4), threshold (i.e. immunity against noise), selection of simple or improved first differentiating filter (see Fig.3), limit for pixel shift range (see Fig.5), common or separate processing of U and V signals, hill protection mode (i.e. no discolourations in narrow colour gaps), low-pass filtering for U and V signals (see Fig.6) and a so called super hill mode, which avoids discolourations in transients within a colour component.

7.3.3 Y-PEAKING

A linear peaking is applied, which amplifies the luminance signal in the middle and the upper ranges of the bandwidth.

The filtering is an addition of:

- The original signal
- The original signal high-passed with maximum gain at frequency = $^1/_2f_s$ (8 MHz)
- The original signal band-passed with centre frequency = $^1/_4f_s$ (4 MHz)
- The original signal band-passed with centre frequency of 2.38 MHz.

The band-passed and high-passed signals are weighted with factors 0, $^1/_{16}$, $^2/_{16}$, $^3/_{16}$, $^4/_{16}$, $^5/_{16}$, $^6/_{16}$, and $^8/_{16}$, resulting in a maximum gain difference of 2 dB at the centre frequencies.

Coring is added to obtain no gain for low amplitudes in the high-pass and band-pass filtered signal, which is considered to be noise. Coring levels can be programmed as 0 (off), ±8, ±16, ±24 to ±120 LSB w.r.t. the (signed) 11-bit filtered signal.

In addition the peaking gain can be reduced depending on the signal amplitude, programming range 0 (no attenuation), $^1/_4$, $^2/_4$, and $^4/_4$. It is also possible to make larger undershoots than overshoots, programming range 0 (no attenuation of undershoots), $^1/_4$, $^2/_4$, and $^4/_4$.

7.3.4 Y-DELAY

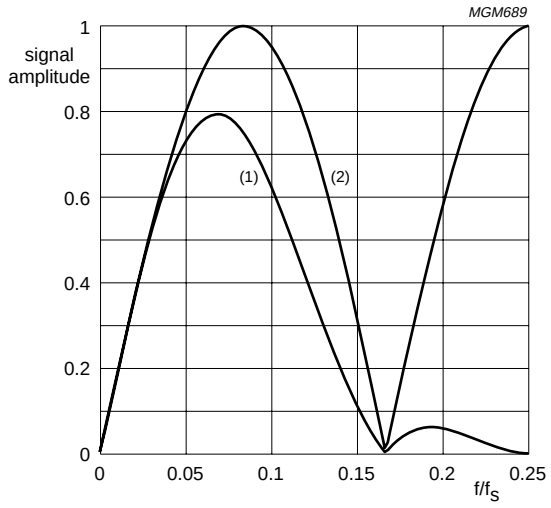
The Y samples can be shifted onto 8 positions w.r.t. the UV samples. This shift is meant to account for a possible difference in delay previous to the SAA4977H. The zero delay setting is suitable for the nominal case of aligned input data. The other settings provide one to seven samples less delay in Y.

7.3.5 SIDEPANELS AND BLANKING

Sidepanels are generated by switching Y and the 4 MSBs of U and V to certain programmable values. The start and stop values for the sidepanels w.r.t. the rising edge of the HRD signal are programmable in a resolution of 4 LLD clock cycles. In addition, a fine shift of 0 to 3 LLD clock cycles of both values can be achieved.

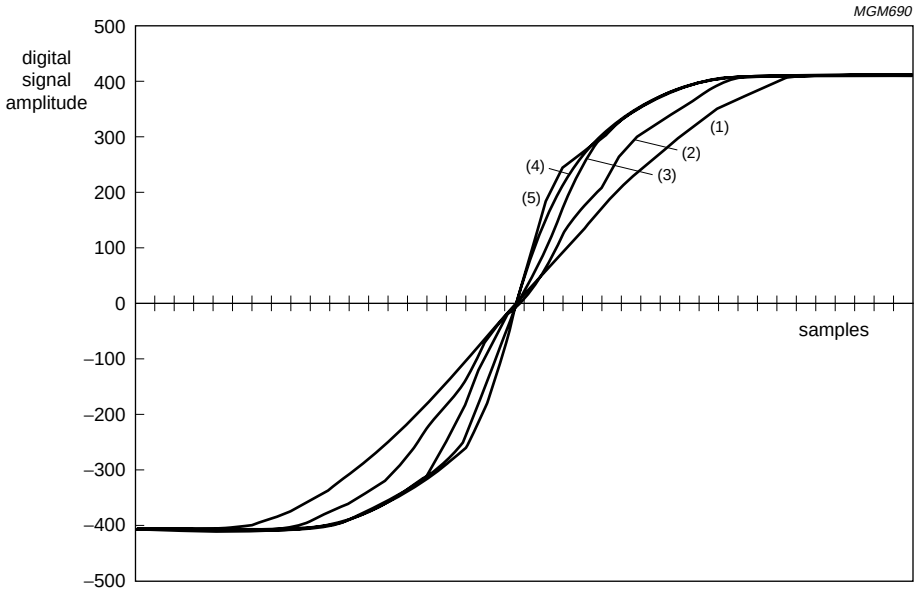
Blanking is done by switching Y to value 64 at 10-bit word and UV to value 0 (in 2's complement). Blanking is controlled by a composite signal HVBDA, consisting of a horizontal part HBDA and a vertical part VBDA. Set and reset value of the horizontal control signal HBDA are programmable w.r.t. the rising edge of the HRD signal, set and reset value of the vertical control signal VBDA are programmable w.r.t. the rising edge of the VA signal.

The range of the Y output signal can be selected between 9 and 10 bits. In the case of 9 bits for the nominal signal there is room left for undershoot and overshoot (adding up to a total of 10 bits). In the case of selecting all 10 bits of the luminance DAC for the nominal signal any under or overshoot will be clipped (see Fig.11).



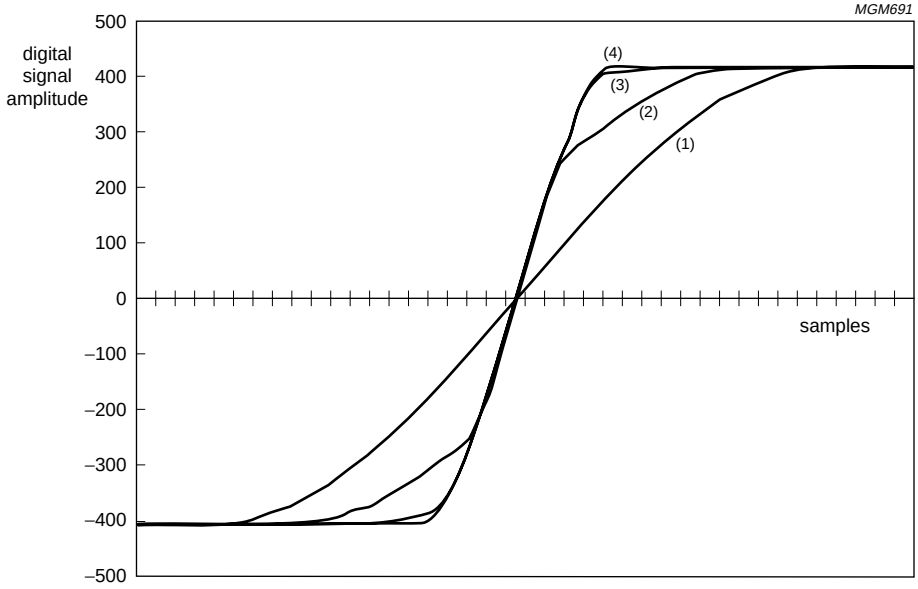
(1) dcti_ddx_sel = 1.
(2) dcti_ddx_sel = 0.

Fig.3 DCTI first differentiating filter; transfer function with variation of control signal dcti_ddx_sel.



(1) input signal.
(2) gain = 1.
(3) gain = 3.
(4) gain = 5.
(5) gain = 7.

Fig.4 DCTI with variation of gain setting (limit = 1).



(1) input signal.
(2) limit = 1.
(3) limit = 2.
(4) limit = 3.

Fig.5 DCTI with variation of limit setting (gain = 7).

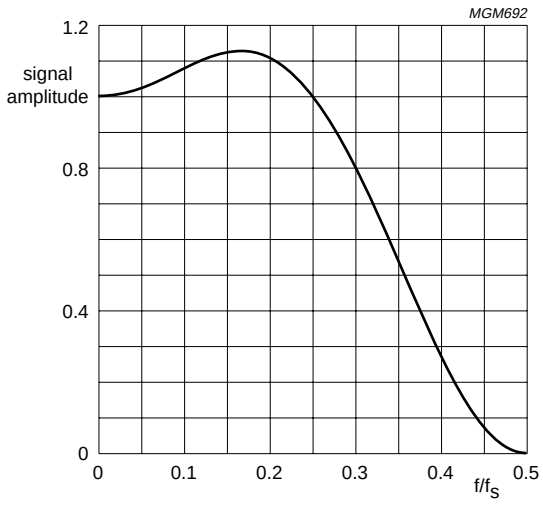
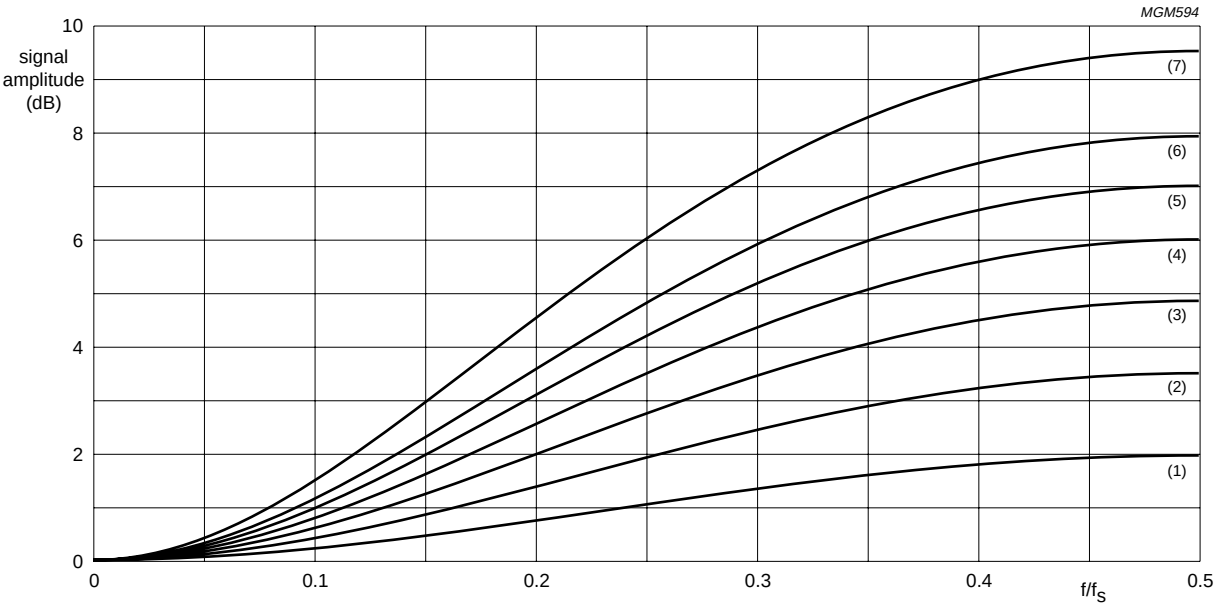
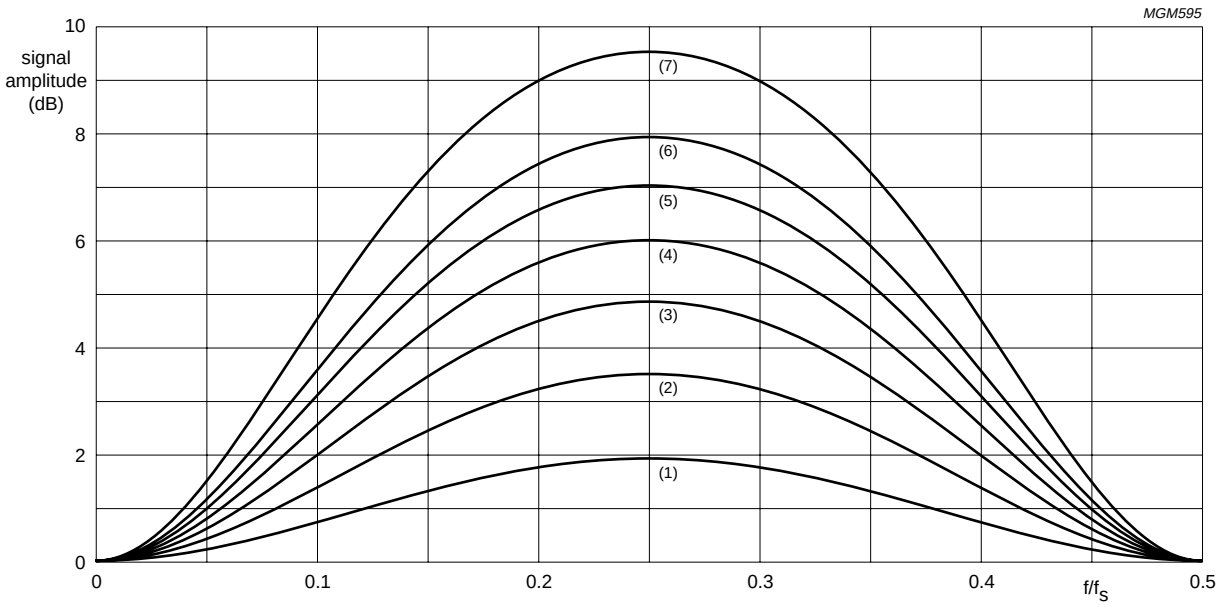


Fig.6 DCTI post-filter transfer function.



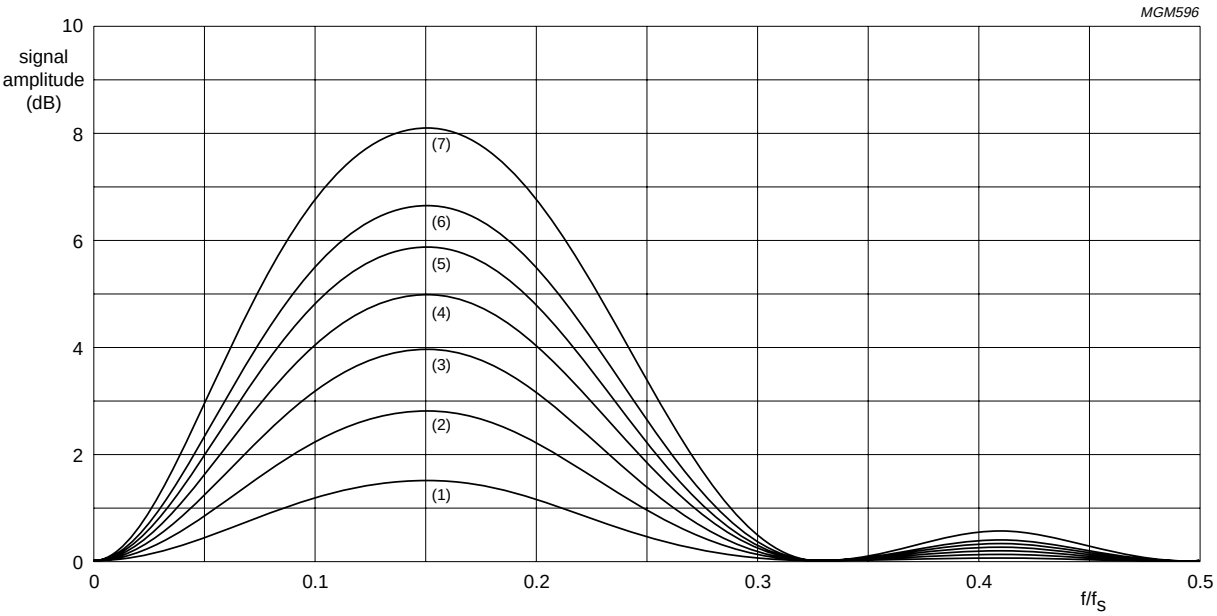
(1) $\beta = 1/16$.
(2) $\beta = 2/16$.
(3) $\beta = 3/16$.
(4) $\beta = 4/16$.
(5) $\beta = 5/16$.
(6) $\beta = 6/16$.
(7) $\beta = 8/16$.

Fig.7 Transfer function of the peaking high-pass filter with variation of β ($\alpha = 0$; $\tau = 0$).



(1) $\alpha = 1/16$.
(2) $\alpha = 2/16$.
(3) $\alpha = 3/16$.
(4) $\alpha = 4/16$.
(5) $\alpha = 5/16$.
(6) $\alpha = 6/16$.
(7) $\alpha = 8/16$.

Fig.8 Transfer function of the peaking band-pass with variation of α ($\beta = 0$; $\tau = 0$).



(1) $\tau = {}^{1}/_{16}$.
(2) $\tau = {}^{2}/_{16}$.
(3) $\tau = {}^{3}/_{16}$.
(4) $\tau = {}^{4}/_{16}$.
(5) $\tau = {}^{5}/_{16}$.
(6) $\tau = {}^{6}/_{16}$.
(7) $\tau = {}^{8}/_{16}$.

Fig.9 Transfer function of peaking low band-pass with variation of τ ($\alpha = 0$; $\beta = 0$).

7.4 Digital-to-analog conversion

Three identical 10-bit DACs are used to map the 4 : 4 : 4 data to analog levels.

7.5 Microprocessor

The SAA4977H contains an embedded 80C51 microprocessor core including a 256 byte RAM and 16 kbyte ROM. The microprocessor runs on a 16 MHz clock, generated by dividing the 32 MHz display clock by a factor of 2. For controlling internal registers a host interface, consisting of a parallel address and data bus, is built-in, that can be addressed as internal AUX RAM via MOVX type of instructions.

7.5.1 I²C-BUS

The I²C-bus interface in the SAA4977H is used in a slave receive and transmit mode for communication with a central system microprocessor. The standardized bus frequencies of both 100 kHz and 400 kHz can be dealt with.

The I²C-bus slave address of the SAA4977H is 0110100 R/$\overline{W}$.

For a detailed description of the transmission protocol refer to brochure *"The I²C-bus and how to use it"* (order number 9398 393 40011) and to Application note *"I²C-bus register specification of the SAA4977H"* (AN98054).

7.5.2 SNERT-BUS

A SNERT interface is built-in, which operates in a master receive and transmit mode for communication with peripheral circuits such as the SAA4990H or SAA4991WP. The SNERT interface replaces the standard UART interface. In contrast to the 80C51 UART interface there are additional special function registers and there is no byte separation time between address and data.

The SNERT interface transforms the parallel data from the microprocessor into 1 Mbaud SNERT data. The SNERT-bus consists of three signals: SNCL used as the serial clock signal and is generated by the SNERT interface; SNDA used as the bidirectional data line, and SNRST used as the reset signal and is generated by the microprocessor to indicate the start of a transmission.

The read or write operation must be set by the microprocessor. When writing to the bus, 2 bytes are loaded by the microprocessor: one for the address, the other for the data.

When reading from the bus, one byte is loaded by the microprocessor for the address, the received byte is the data from the addressed SNERT location.

7.5.3 I/O PORTS

A parallel 8-bit I/O port (P1) is available, where P1.0 is used as the SNERT reset signal (SNRST), P1.1 to P1.5 can be used for application specific control signals, and P1.6 and P1.7 are used as I²C-bus signals (SCL and SDA).

7.5.4 WATCHDOG TIMER

The microprocessor contains an internal Watchdog Timer, which can be activated by setting the bit 4 in SFR PCON. Only a synchronous reset will clear this bit. To prevent a system reset the Watchdog Timer must be reloaded in time. The Watchdog Timer is incremented every 0.75 ms. The time interval between the timer's reloading and the occurrence of a reset depends on the reloaded 8-bit value.

7.5.5 RESET

A reset is accomplished by holding the RST pin HIGH for at least 0.75 μs while the external clock is running.

To guarantee reliable power-up behaviour the reset pulse must not be performed until V_{DD} is stabilized and the external clock is running.

7.6 Memory controller

The memory controller provides all necessary acquisition clock related write signals (WE and RSTW) and display clock related read signals (RE and IE2) to control one or two-field memory concepts. Furthermore the drive signals (HDFL and VDFL) for the horizontal and vertical deflection power stages are generated. Also a horizontal blanking pulse BLND is generated which can be used for peripheral circuits as SAA4990H. The memory controller is connected to the microprocessor via the host interface. Start and stop values for all pulses, referring to the corresponding horizontal or vertical reference signal, are programmable under control of the internal software. To allow user access to these control signals via the I²C-bus a range of subaddresses is reserved; for a detailed description of this user interface refer to Application Note *"I²C-bus register specification of the SAA4977H"* (AN98054).

7.6.1 WE

The write enable signal for field memory 1 is a composite signal consisting of a horizontal and a vertical part. The horizontal position w.r.t the rising edge of the HA signal and the vertical position w.r.t the rising edge of the VA signal are programmable.

7.6.2 RSTW

Reset write signal for field memory 1; this signal is derived from the positive edge of the VA input signal and has a pulse width of 64 μs.

7.6.3 RE

The read enable signal for field memory 1 is a composite signal consisting of a horizontal and a vertical part. The horizontal position w.r.t the rising edge of the HA signal and the vertical position w.r.t the rising edge of the VA signal are programmable.

7.6.4 IE2

Input enable signal for field memory 2, can be directly set or reset by the microprocessor.

7.6.5 HDFL

Horizontal deflection signal for driving a deflection circuit; this signal has a cycle time of 32 μs and a pulse width of 76 LLD clock cycles.

7.6.6 VDFL

Vertical deflection signal for driving a deflection circuit; this signal has a cycle time of 10 ms; the start and stop value w.r.t the rising edge of the VA signal is programmable in steps of 16 μs.

7.6.7 BLND

Horizontal blanking signal for peripheral circuits e.g. SAA4990H, start and stop values w.r.t. the rising edge of HRD are programmable.

7.7 Line locked clock generation

7.7.1 Phase comparison of HA rising edge with generated H_{ref} signal

The HA signal, which has a nominal period of 64 μs, is used as a timing reference for the line locked acquisition clock system. This HA signal may vary in position from application to application, related to the active video part.

The phase comparator measures the delay between the HA and the internally generated, clock synchronous H_{ref} signal.

7.7.2 PLL clock generator running at 32 MHz (2048 clock cycles per line)

The basic frequency of the clock generator is 32 MHz. The type of PLL is known as ‘Petra PLL’. This is a purely analog clock generator, with analog frequency control via a loop filter on the measured phase error.

7.7.3 Divide-by-2 for master clock 16 MHz

A simple clock divider is used to generate 16 MHz out of 32 MHz. The advantage of this construction is the inherent 50% duty cycle on the acquisition clock.

7.7.4 Divide by another 1024 to generate line frequent, clock synchronous H_{ref} signal

The video lines contain 1024 clock cycles of 16 MHz. Therefore, frequency division by 1024 creates a 50% duty cycle line frequent signal H_{ref}.

7.8 Clock and sync interfacing

Typically the circuit operates as a two clock system, i.e. LLA is supplied with a 16 MHz clock and LLD with a 32 MHz clock.

The line locked display clock LLD must be provided by the application. Also a line frequent signal must be provided by the application at pin HA. A vertical 50 or 60 Hz synchronization signal has to be applied on pin VA.

It is also possible to use an external line locked acquisition clock, which must be provided at pin LLA. This operation mode can be selected by the SELCLK pin. When using the external acquisition clock the HA signal must be synchronous to the acquisition clock.

A display clock synchronous line frequent signal is put out at pin HRD providing a duty factor of 50%. The rising edge of HRD is also the reference for display related control signals as BLND, RE, HDAV and HBDA.

The acquisition clock is buffered internally and put out as serial write clock (SWC) for supplying the field memory.

7.9 4 : 1 : 1 I/O interfacing

Table 2 Digital input and output bus format

OUTPUT PIN	4 : 1 : 1 FORMAT				INPUT PIN
YO7	Y07	Y17	Y27	Y37	YI7
YO6	Y06	Y16	Y26	Y36	YI6
YO5	Y05	Y15	Y25	Y35	YI5
YO4	Y04	Y14	Y24	Y34	YI4
YO3	Y03	Y13	Y23	Y33	YI3
YO2	Y02	Y12	Y22	Y32	YI2
Y01	Y01	Y11	Y21	Y31	YI1
YO0	Y00	Y10	Y20	Y30	YI0
UVO7	U07	U05	U03	U01	UVI7
UVO6	U06	U04	U02	U00	UVI6
UVO5	V07	V05	V03	V01	UVI5
UVO4	V06	V04	V02	V00	UVI4

The first phase of the 4 : 1 : 1 YUV dataword is available on the output bus one SWC clock cycle after the rising edge of the WE signal. The start position, when the first phase of the 4 : 1 : 1 YUV data word is expected on the input bus, can be defined by the internal control signal HDAV.

The luminance output signal is in 8-bit straight binary format, whereas U and V output signals are in 2's complement format. Also the luminance input signal is expected in 8-bit straight binary format, whereas U and V input signals are expected in 2's complement format. The U and V input signals are inverted if the corresponding control bit uv_inv is set via the I^2C-bus.

7.10 Test mode operation

The SAA4977H provides a test mode function which should not be entered by the customer. If the $\overline{\text{TRST}}$ input is driven HIGH, different test modes can be selected by applying a HIGH to the TMS input for a defined number of LLD clock cycles. To exit the test mode TMS and $\overline{\text{TRST}}$ must be driven LOW.

7.11 I²C-bus control registers

ADDRESS	BIT	NAME	DESCRIPTION
Subaddress 00H to 2FH: reserved; note 1			
Subaddress 30H to 32H (AGC)			
30H	0 to 7	AGC_Y	AGC gain for Y channel (2's complement relative to 0 dB): upper 8 bits
31H	0 to 7	AGC_UV	AGC gain for U and V channel (2's complement relative to 0 dB): upper 8 bits
32H	0	AGC_Y	AGC gain for Y channel LSB
	1	AGC_UV	AGC gain for UV channel LSB
	2	standby_f	front-end in standby mode if HIGH
	3	aaf_bypass	bypass for prefilter if HIGH
	4 to 7	–	reserved
Subaddress 33H (UV clamp correction)			
33H	0 and 1	UVclcor_mode	clamp correction mode = auto, fixed, keep, reserved
	2 to 4	Uclcor_fval	fixed value for clamp correction U channel
	5 to 7	Vclcor_fval	fixed value for clamp correction V channel
Subaddress 34H (UV coring)			
34H	0 and 1	UVcoring	coring level = 0, ±0.5, ±1 and ±2 LSB
	2 and 3	–	reserved
	4 and 5	UVcl_tau	vertical filtering of measured clamp
	6 and 7	–	reserved
Subaddress 35H (Y delay)			
35H	0 to 2	ydelay_f	variable Y-delay in LLA clock cycles: –4, –3, –2, –1, 0, 1, 2 and 3
	3 and 4	overl_thr	overload threshold: (216, 224, 232, 240)
	5	fill_mem	fill memory with constant value if HIGH
	6 and 7	–	reserved
Subaddress 36H and 37H (DCTI)			
36H	0 to 2	dcti_gain	DCTI gain: 0, 1, 2, 3, 4, 5, 6 and 7
	3 to 6	dcti_threshold	DCTI threshold: 0, 1 to 15
	7	dcti_ddx_sel	DCTI selection of first differentiating filter; see Fig.3
37H	0 and 1	dcti_limit	DCTI limit for pixel shift range: 0, 1, 2 and 3
	2	dcti_separate	DCTI separate processing of U and V signals; 0 = off, 1 = on
	3	dcti_protection	DCTI over the hill protection; 0 = off, 1 = on
	4	dcti_filteron	DCTI post-filter; 0 = off, 1 = on
	5	dcti_superhill	DCTI super hill mode; 0 = off, 1 = on
	6 and 7	–	reserved
Subaddress 38H and 3AH (peaking)			
38H	0 to 2	pk_alpha	peaking alpha: $\frac{1}{16}$ (0, 1, 2, 3, 4, 5, 6, 8)
	3 to 5	pk_beta	peaking beta: $\frac{1}{16}$ (0, 1, 2, 3, 4, 5, 6, 8)
	6 and 7	–	reserved

ADDRESS	BIT	NAME	DESCRIPTION
39H	0 to 2	pk_tau	peaking tau: $\frac{1}{16}$ (0, 1, 2, 3, 4, 5, 6, 8)
	3 and 4	pk_delta	peaking amplitude dependent attenuation: $\frac{1}{4}$ (0, 1, 2, 4)
	5 and 6	pk_neggain	peaking attenuation of undershoots: $\frac{1}{4}$ (0, 1, 2, 4)
	7	–	reserved
3AH	0 to 3	pk_corthr	peaking coring threshold 0, ±8, ±16 to ±120 LSB
	4 to 7	–	reserved
Subaddress 3BH and 3CH (sidepanels overlay)			
3BH	0 to 3	overlay_u	sidepanels overlay U (4 MSB)
	4 to 7	overlay_v	sidepanels overlay V (4 MSB)
3CH	0 to 7	overlay_y	sidepanels overlay Y (8 MSB)
Subaddress 3DH to 3FH (sidepanel position)			
3DH	0 to 7	sidepanel_start	sidepanel start position (8 MSB) w.r.t. the rising edge of HRD signal
3EH	0 to 7	sidepanel_stop	sidepanel stop position (8 MSB) w.r.t. the rising edge of HRD signal
3FH	0 and 1	sidepanel_fdel	fine delay of sidepanel signal in LLD clock cycles: 0, 1, 2 and 3
	2	output_range	output range (output range = 0: 9 bit for the nominal output signal, black level: 288 and white level: 767; output range = 1: 10 bit for the nominal output signal, black level 64 and white level 1023)
	3	uv_inv	inverts UV input signals: 0 = no inversion, 1 = inversion
	4 to 6	ydelay_out	variable Y-delay in LLD clock cycles: –7, –6, –5, –4, –3, –2, –1 and 0
	7	–	reserved

Note

1. Detailed information about the software dependent I^{2}C-bus registers can be found in Application Note *"I^{2}C-bus register specification of the SAA4977H"* (AN98054).

8 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{DDA(1,2,3)}$	analog supply voltage front-end		–0.5	+5.5	V
$V_{DDD(1,2,3)}$	digital supply voltage front-end		–0.5	+5.5	V
$V_{DDA(4,5)}$	analog supply voltage back-end		–0.5	+3.6	V
$V_{DDD(4,5,6)}$	digital supply voltage back-end		–0.5	+3.6	V
V_{DDIO}	digital I/O supply voltage back-end		–0.5	+5.5	V
V_I	input voltage for all digital input pins		–0.5	+5.5	V
V_I	input voltage for all digital I/O pins	V_{DDIO} = 5.0 V	–0.5	+5.5	V
		V_{DDIO} = 3.3 V	–0.5	+3.8	V
T_{stg}	storage temperature		–20	+150	°C
T_{amb}	operating ambient temperature		–20	+60	°C

9 THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	50	K/W

10 CHARACTERISTICS

$V_{DDD(1,2,3)}$ = 4.75 to 5.25 V; $V_{DDA(1,2,3)}$ = 4.75 to 5.25 V; $V_{DDD(4,5,6)}$ = 3.15 to 3.45 V; $V_{DDA(4,5)}$ = 3.15 to 3.45 V; V_{DDIO} = 4.75 to 5.25 V; T_{amb} = 0 to 60 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
$V_{DDA(1,2,3)}$	analog supply voltage front-end		4.75	5.0	5.25	V
$V_{DDD(1,2,3)}$	digital supply voltage front-end		4.75	5.0	5.25	V
$I_{DDA(1,2,3)}$	analog supply current front-end		–	85	100	mA
$I_{DDD(1,2,3)}$	digital supply current front-end		–	65	80	mA
$V_{DDA(4,5)}$	analog supply voltage back-end		3.15	3.3	3.45	V
$V_{DDD(4,5,6)}$	digital supply voltage back-end		3.15	3.3	3.45	V
V_{DDIO}	I/O supply voltage back-end		3.15	5.0	5.25	V
$I_{DDA(4,5)}$	analog supply current back-end		–	25	35	mA
$I_{DDD(4,5,6)}$	digital supply current back-end		–	40	55	mA
I_{DDIO}	I/O supply current back-end		–	1	10	mA
Dissipation						
P_{tot}	total power dissipation		–	–	1.3	W
Luminance input signal (Y clamp level digital 16)						
$V_{i(p-p)}$	Y input level (peak-to-peak value)	AGC fixed at 0 dB; note 1	0.95	1.00	1.05	V
C_i	input capacitance		–	7	15	pF
I_{LI}	input leakage current	clamp not active	–	–	100	nA
I_I	input current	during clamping	–	–	±150	μA
$\alpha_{AGC(max)}$	maximum AGC attenuation		5.75	6	–	dB
$G_{AGC(max)}$	maximum AGC gain		5.75	6	–	dB
$\alpha_{AGC(acc)}$	AGC attenuation accuracy digital		–	8	–	bits
$G_{AGC(acc)}$	AGC gain accuracy digital		–	8	–	bits
Colour difference input signals (U and V clamp level digital 128)						
$V_{i(p-p)}$	U input level (peak-to-peak value)	AGC fixed at 0 dB; note 1	1.29	1.34	1.39	V
	V input level (peak-to-peak value)	AGC fixed at 0 dB; note 1	1.00	1.05	1.10	V
C_i	input capacitance		–	–	15	pF
I_{LI}	input leakage current	clamp not active	–	–	100	nA
I_I	input current	during clamping	–	–	±150	μA
$\alpha_{AGC(max)}$	maximum AGC attenuation		5.75	6	–	dB
$G_{AGC(max)}$	maximum AGC gain		5.75	6	–	dB
$\alpha_{AGC(acc)}$	AGC attenuation accuracy digital		–	8	–	bits
$G_{AGC(acc)}$	AGC gain accuracy digital		–	8	–	bits

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Analog input transfer function (sample rate 16 MHz/8 bits)						
f_{CLK}	maximum sample clock		18	–	–	MHz
INL	integral non linearity	ramp input signal	–1	–	+1	LSB
DNL	differential non linearity	ramp input signal	–0.75	–	+0.75	LSB
S/N	signal-to-noise ratio	nominal amplitude; 0 to 8 MHz	43	–	–	dB
HD	harmonic distortion (2nd to 5th harmonic)	95% amplitude; Y at 4.3 MHz; UV at 1 MHz	–	–50	–37	dB
G_{dif}	differential gain	f_{CLK} = 4.4 MHz; ADC only; at nominal AGC setting	–	1	2	%
SVR	supply voltage rejection	note 2	34	–	–	dB
Analog Y, U and V input filter (third order linear phase filter with notch at f_{CLK})						
$f_{(-3dB)}$	3 dB down frequency	f_{CLK} = 16 MHz	5.4	5.6	5.8	MHz
$\alpha_{(0.5)}$	attenuation at $\frac{1}{2}f_{CLK}$ (8 MHz)		7	8	–	dB
α_{sb}	stop band attenuation		30	–	–	dB
f_{notch}	notch frequency		15.5	16	16.5	MHz
$t_{d(g)}$	group delay	f_{CLK} = 4 MHz	–	55	65	ns
$t_{d(g)(dif)}$	differential group delay within 1 to 6 MHz		–	20	30	ns
Luminance output signal (output_range = 0: Y black level digital 288, white level digital 767, output_range = 1: Y black level digital 64, white level digital 1023); see Fig.11						
$V_{o(p-p)}$	Y output level (peak-to-peak value)	Z_L = 2 kΩ	1.28	1.34	1.40	V
R_o	output resistance		–	50	100	Ω
R_L	resistive load		1	2	–	kΩ
C_L	capacitive load		–	–	25	pF
SVR	supply voltage rejection	note 2	34	–	–	dB
α_{ct}	crosstalk attenuation between outputs	0 to 10 MHz	40	–	–	dB
S/N	signal-to-noise ratio	nominal amplitude; 0 to 10 MHz	46	–	–	dB
Colour difference output signals (U and V digital range 0 to 1023)						
$V_{o(p-p)}$	U output level (peak-to-peak value)	Z_L = 2 kΩ	1.28	1.34	1.40	V
	V output level (peak-to-peak value)	Z_L = 2 kΩ	1.28	1.34	1.40	V
$G_{m(U-V)}$	gain matching U to V		–	1	3	%
R_o	output resistance		–	50	100	Ω
R_L	resistive load		1	2	–	kΩ
C_L	capacitive load		–	–	25	pF
SVR	supply voltage rejection	note 2	34	–	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
α_{ct}	crosstalk attenuation between outputs	0 to 10 MHz	40	–	–	dB
S/N	signal-to-noise ratio	nominal amplitude; 0 to 10 MHz	46	–	–	dB
Output transfer function (sample rate 32 MHz/10 bits)						
INL	integral non linearity		–2	–	+2	LSB
DNL	differential non linearity		–1	–	+1	LSB
Digital output signals: YO, UVO, WE and RSTW (C_L = 15 pF); timing referred to SWC clock						
V_{OH}	HIGH-level output voltage	I_{OH} = –2.0 mA	2.4	–	–	V
V_{OL}	LOW-level output voltage	I_{OL} = 1.6 mA	–	–	0.4	V
$t_{d(o)}$	output delay time	see Fig.10	–	–	20	ns
$t_{h(o)}$	output hold time	see Fig.10	4	–	–	ns
Digital output signal: SWC (C_L = 15 pF); timing referred to LLA clock						
V_{OH}	HIGH-level output voltage	I_{OH} = –2.0 mA	2.4	–	–	V
V_{OL}	LOW-level output voltage	I_{OL} = 1.6 mA	–	–	0.4	V
$t_{d(o)}$	output delay time	see Fig.10	3	–	12	ns
Digital output signal: HRD						
V_{OH}	HIGH-level output voltage	I_{OH} = –2.0 mA	2.4	–	–	V
V_{OL}	LOW-level output voltage	I_{OL} = 1.6 mA	–	–	0.4	V
Digital output signals: IE2, BLND, RE, HDFL and VDFL (C_L = 15 pF); timing referred to LLD clock						
V_{OH}	HIGH-level output voltage	I_{OH} = –2.0 mA	2.4	–	–	V
V_{OL}	LOW-level output voltage	I_{OL} = 1.6 mA	–	–	0.4	V
$t_{d(o)}$	output delay time	see Fig.10	–	–	20	ns
$t_{h(o)}$	output hold time	see Fig.10	4	–	–	ns
Digital input/output signals: P1.1 to P1.5 and SNRST						
V_{OH}	HIGH-level output voltage	I_{OH} = –0.06 mA	2.4	–	–	V
V_{OL}	LOW-level output voltage	I_{OL} = 1.6 mA	0	–	0.4	V
V_{IH}	HIGH-level input voltage		2.0	–	V_{DDIO} + 0.3	V
V_{IL}	LOW-level input voltage		0	–	0.8	V
Digital input signals: YI and UVI; timing referred to LLD clock						
V_{IH}	HIGH-level input voltage		2.0	–	5.5	V
V_{IL}	LOW-level input voltage		–	–	0.8	V
$t_{su(i)}$	input set-up time	see Fig.10	4	–	–	ns
$t_{h(i)}$	input hold time	see Fig.10	3	–	–	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Digital input signal: HA; timing referred to LLA clock (only when SELCLK = 0, HA used as digital horizontal reference)						
V_{IH}	HIGH-level input voltage		2.0	–	5.5	V
V_{IL}	LOW-level input voltage		–	–	0.8	V
$t_{su(i)}$	input set-up time	see Fig.10	7	–	–	ns
$t_{h(i)}$	input hold time	see Fig.10	4	–	–	ns
Digital input signals: $\overline{TRST}$, TMS, RST and VA						
V_{IH}	HIGH-level input voltage		2.0	–	5.5	V
V_{IL}	LOW-level input voltage		–	–	0.8	V
Digital input clock signal: LLA						
f_{LLA}	sample clock frequency		14	16	34	MHz
δ_{clk}	clock duty factor		40	50	60	%
V_{IH}	HIGH-level input voltage		2.4	–	–	V
V_{IL}	LOW-level input voltage		–	–	0.6	V
t_r	clock rise time	see Fig.10	–	–	5	ns
t_f	clock fall time	see Fig.10	–	–	5	ns
Digital input clock signal: LLD						
f_{LLD}	sample clock frequency		30	32	34	MHz
δ_{clk}	clock duty factor		40	50	60	%
V_{IH}	HIGH-level input voltage		2.4	–	–	V
V_{IL}	LOW-level input voltage		–	–	0.6	V
t_r	clock rise time	see Fig.10	–	–	5	ns
t_f	clock fall time	see Fig.10	–	–	5	ns
I^2C-bus signal: SDA and SCL; note 3						
V_{IH}	HIGH-level input voltage		$0.7V_{DDIO}$	–	–	V
V_{IL}	LOW-level input voltage		–	–	$0.3V_{DDIO}$	V
V_{OL}	LOW-level output voltage	I_{OL} = 3.0 mA	–	–	0.4	V
f_{SCL}	SCL clock frequency		–	–	400	kHz
$t_{HD;STA}$	hold time START condition		0.6	–	–	µs
t_{LOW}	SCL LOW time		1.3	–	–	µs
t_{HIGH}	SCL HIGH time		0.6	–	–	µs
$t_{SU;DAT}$	data set-up time		100	–	–	ns
$t_{SU;DAT1}$	data set-up time (before repeated START condition)		0.6	–	–	µs
$t_{SU;DAT2}$	data set-up time (before STOP condition)		0.6	–	–	µs
$t_{SU;STA}$	set-up time repeated START		0.6	–	–	µs
$t_{SU;STO}$	set-up time STOP condition		0.6	–	–	µs

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
SNERT-bus: SNDA and SNCL; note 4						
V_{OH}	HIGH-level output voltage	I_{OH} = –2.0 mA	2.4	–	–	V
V_{OL}	LOW-level output voltage	I_{OL} = 1.6 mA	–	–	0.4	V
V_{IH}	HIGH-level input voltage		2.0	–	V_{DDIO} + 0.3	V
V_{IL}	LOW-level input voltage		–	–	0.8	V
$t_{su(i)}$	input set-up time		700	–	–	ns
$t_{h(i)}$	input hold time		0	–	–	ns
t_{cycle}	SNCL cycle time		–	1	–	µs
$t_{h(o)}$	output hold time		50	–	–	ns

Notes

1. With AGC at –3 dB, U full ADC range is obtained at V_i = 1.89 V; with AGC at +6 dB, U full ADC range is obtained at V_i = 0.67 V; with AGC at –3 dB, V full ADC range is obtained at V_i = 1.48 V; with AGC at +6 dB, V full ADC range is obtained at V_i = 0.52 V.
2. Supply voltage ripple rejection, measured over a frequency range from 20 Hz to 50 kHz. This includes $\frac{1}{2}f_V$, f_V, $2f_V$, f_H and $2f_H$ which are major load frequencies: SVR is relative variation of the full scale analog input for a supply variation of 0.25 V.
3. The AC characteristics are in accordance with the I²C-bus specification for fast mode (clock frequency maximum 400 kHz). Information about the I²C-bus can be found in the brochure *"I²C-bus and how to use it"* (order number 9398 393 40011).
4. More information about the SNERT-bus protocol can be found in Application Note *"The SNERT-bus specification"* (AN95127).

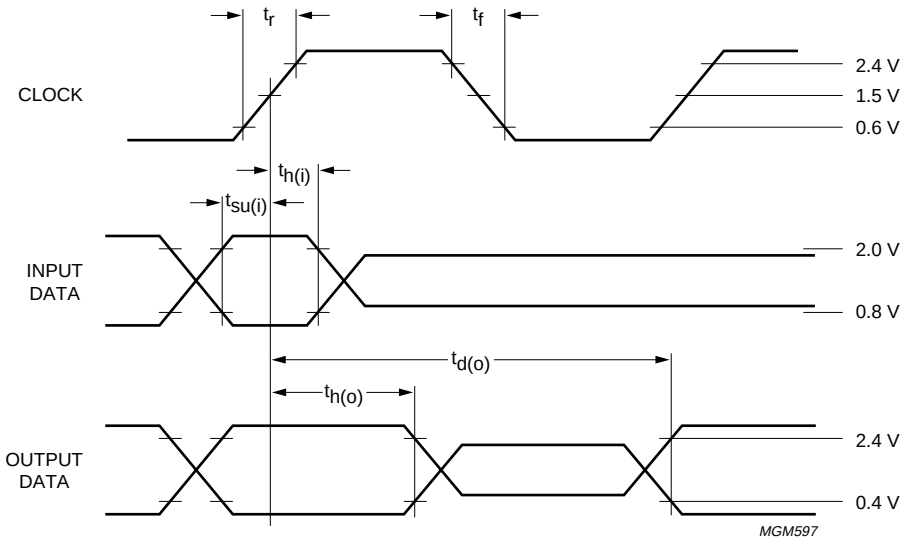


Fig.10 Timing diagram.

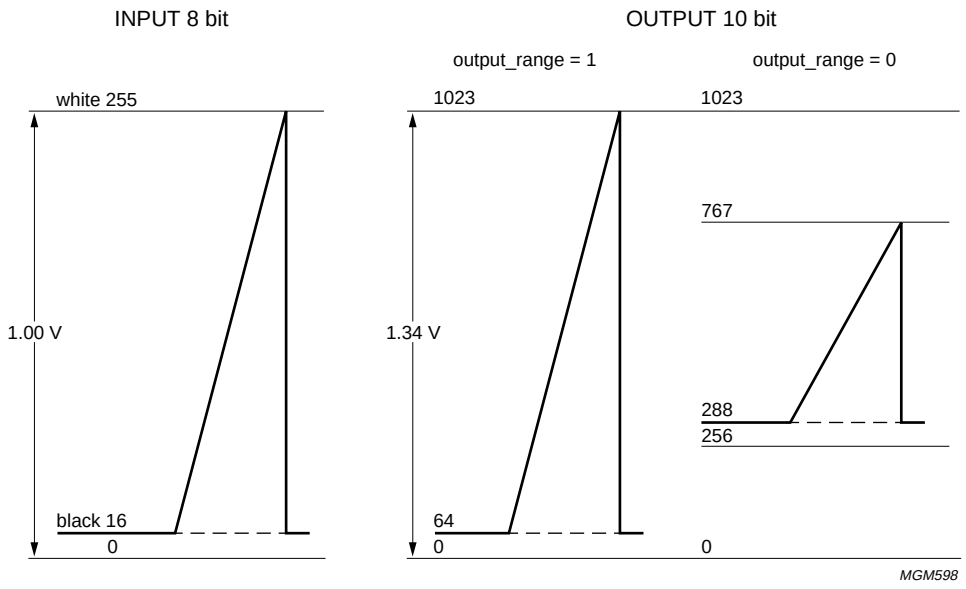


Fig.11 Luminance levels.

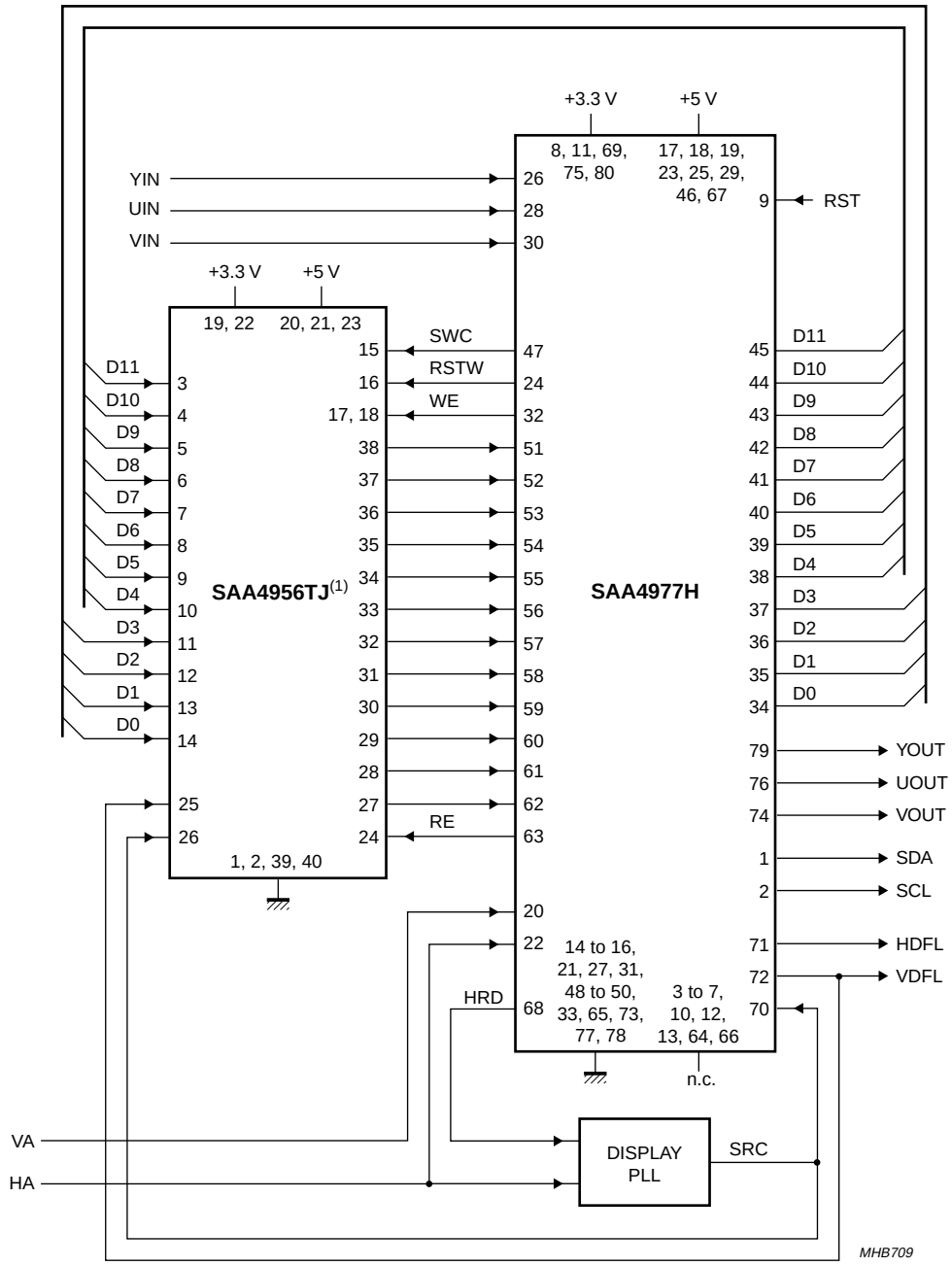
11 APPLICATION

The SAA4977H supports two different up-converter concepts. The simple one is shown in Fig.12. In this application only one field memory SAA4955TJ is needed for a 100 Hz conversion based on a field repetition algorithm (AABB mode). The concept can be upgraded by a noise reduction based on a motion adaptive field recursive filter if the SAA4956TJ is used instead of the SAA4955TJ.

The SAA4977H supports a dual-clock system. The acquisition clock is taken from the digital front-end. The display control is based on a clock generated by an external H-PLL. By this structure the stability of the display is enhanced compared to a one-clock system if an unstable source like a VCR is used as an input.

The second system supported by the SAA4977H is shown in Fig.13. This concept needs two field memories (SAA4955TJ) and the signal processing IC MELZONIC (SAA4991WP). The SAA4991WP allows a vector based motion estimation and compensation for a display of 100 Hz pictures in high-end TV sets which is free of motion artefacts.

It additionally provides a variable vertical zoom function, noise and cross colour reduction. Furthermore a multi-PIP feature is supported making use of the field memories.



(1) Alternatively SAA4955TJ.

Fig.12 Application diagram 1.

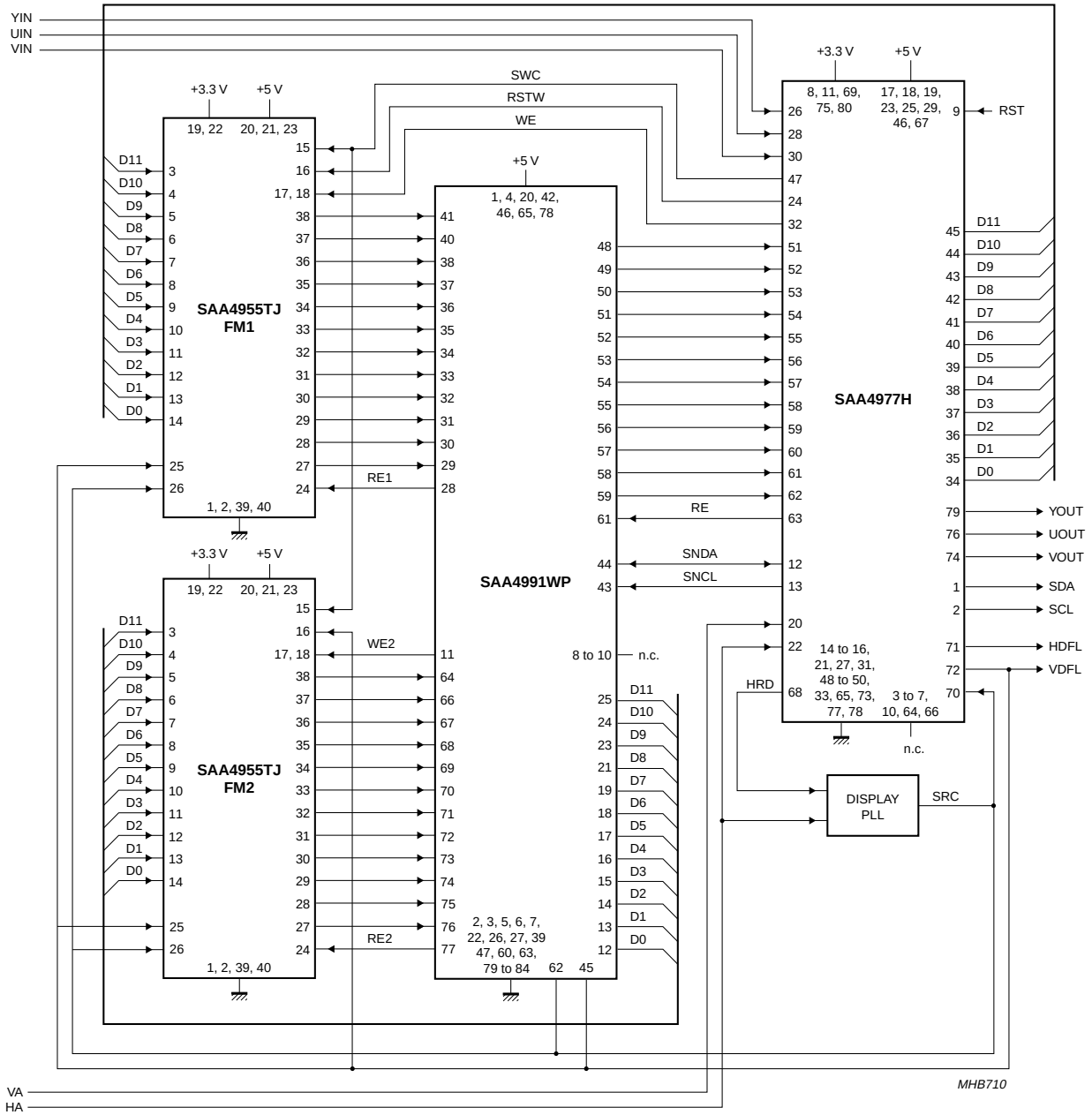
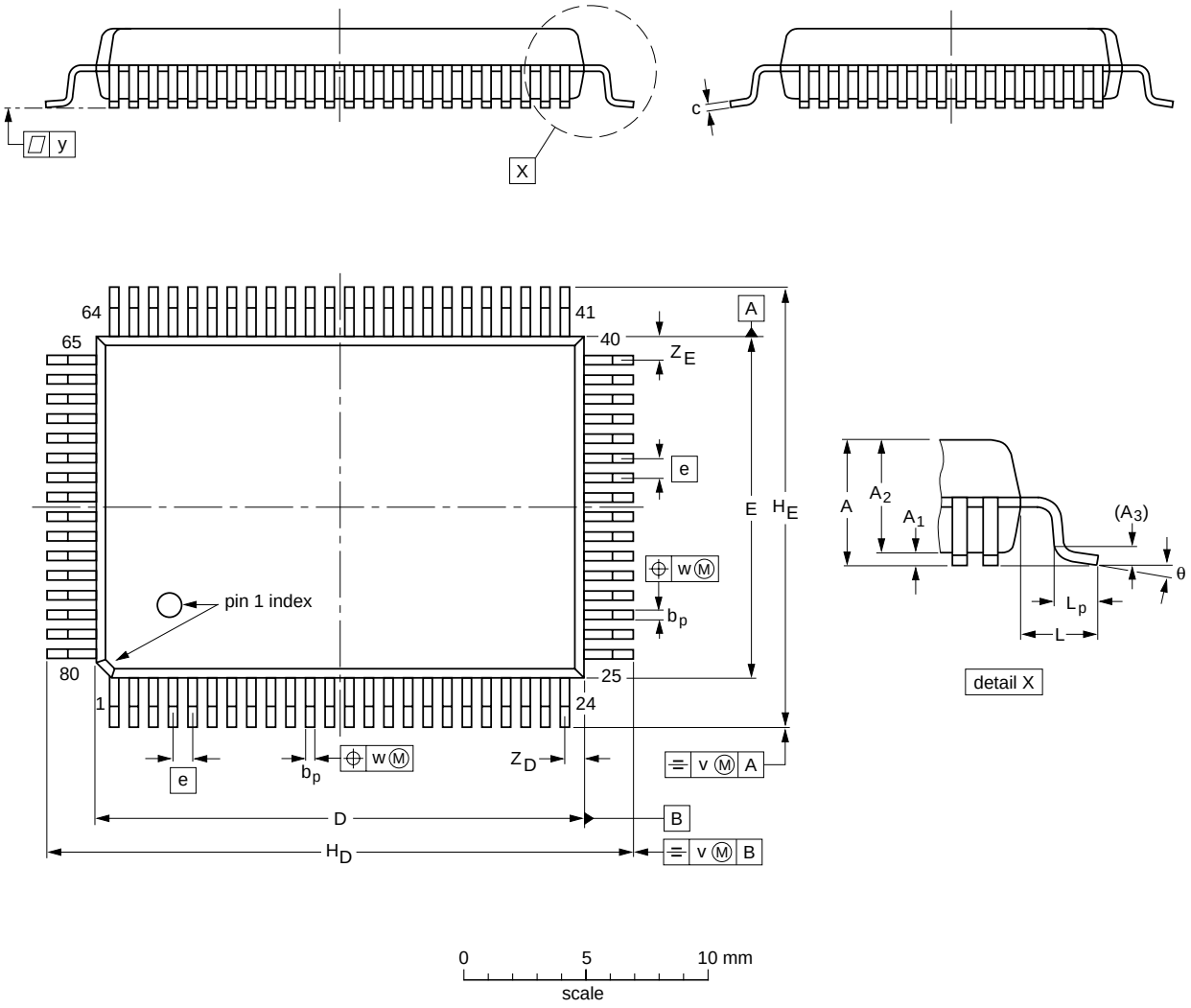


Fig.13 Application diagram 2.

12 PACKAGE OUTLINE

QFP80: plastic quad flat package; 80 leads (lead length 1.95 mm); body 14 x 20 x 2.8 mm **SOT318-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	3.2	0.25 0.05	2.90 2.65	0.25	0.45 0.30	0.25 0.14	20.1 19.9	14.1 13.9	0.8	24.2 23.6	18.2 17.6	1.95	1.0 0.6	0.2	0.2	0.1	1.0 0.6	1.2 0.8	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT318-2		MO-112				~~97-08-01~~ 99-12-27

13 SOLDERING

13.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

13.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 230 °C.

13.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

13.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

13.5 Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW(1)
BGA, LFBGA, SQFP, TFBGA	not suitable	suitable
HBCC, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, SMS	not suitable(2)	suitable
PLCC(3), SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended(3)(4)	suitable
SSOP, TSSOP, VSO	not recommended(5)	suitable

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

14 DATA SHEET STATUS

DATA SHEET STATUS	PRODUCT STATUS	DEFINITIONS (1)
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

Note

1. Please consult the most recently issued data sheet before initiating or completing a design.

15 DEFINITIONS

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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